

REMARKS/ARGUMENTS

The Applicant originally submitted Claims 1-20 in the Application. The Applicant has amended independent Claims 1, 8 and 15 for purposes of clarification only, and has not added any new matter. Dependent Claims 3, 10 and 17 have been amended for reasons of dependency. Accordingly, Claims 1, 3-8, 10-15, and 17-20 are currently pending in the Application.

I. Rejection of Claims 1, 3-8, 10-15 and 17-20 under 35 U.S.C. § 103

The Examiner has rejected Claims 1, 3-8, 10-15 and 17-20 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Application No. 2002/0085578 A1 to Dell, *et al.* ("Dell") in view of U.S. patent No. 6,667,983 B1 to Lo, *et al.* ("Lo") and U.S. Patent No. 6,963,576 to Lee ("Lee").

Amended Claim 1 is directed to a head blockage avoidance system. The system includes a priority summarizer configured to generate a priority summary of the packets within the *m* inputs and the *n* packet FIFOs. The *n* packet FIFOs occupy a same hierarchical level. The priority summarizer indicates which of the *n* packet FIFOs contains *and is to receive* a highest priority packet from one of the *m* inputs. The head avoidance blockage system further comprises a scheduler configured to cause packets in the *n* packet FIFOs to be queued for processing based on the priority summary such that packets in a packet FIFO that contains or is to receive said highest priority packets are triggered to be processed before packets in other of said *n* packet FIFOs. (Emphasis added.)

As discussed in the previous Amendment of May 21, 2007, Dell is directed to a switching stage that employs crossbar devices. (See page 2, paragraph [0013].) In Dell, the "switch fabric of

the present invention is a cell-switching engine handling fixed-sized switching cells.” (See page 6, paragraph [0090].) Dell uses one or more crossbars to achieve scalability in self-routing of cells. (See page 2, paragraph [0012].)

As was also discussed in the previous Amendment of May 21, 2007, Lo is directed to a scalable arbiter for arbitrating between multiple FIFO entry points of a network interface card. (See Abstract.) Lee is directed toward an arbitration scheme that is used for scheduling connections between input ports and output ports.

The Examiner cites Dell for the proposition that:

Dell at al further discloses summarizing priority of packets from FIFOs, indicating which of the packets contains or is to receive a highest priority, and scheduling the packets for processing based on the summarized priority such that packets in a packet FIFO that contain the highest priority are triggered to be processed before packets in other FIFOs (See page 8, paragraph 107 and page 10 paragraphs 145-153 of Dell et al. for reference to an arbiter receiving bids summarizing packet priority from packets of the FIFOs and for reference to arbitrating between packets based on priority such that packets in a FIFO *that contain the highest priority are always processed before packets in other FIFOs*). (See Examiner's Action, page 3; emphasis added.)

In the invention of Claim 1, however, unlike the cited references, priority summarizes is configured to generate a priority summary of the packets within the m inputs and n packet FIFOs that indicates which of the n packet FIFOs contains *and is to receive* a highest priority packet from one of the m inputs...

In the present Application, in one embodiment:

[0044] ... [A]dditionally, the head of line blockage avoidance system 300 includes a scheduler 360. The scheduler 360 is configured to cause one of the packet FIFOs 330, 332, 340, 342 to be queued for processing based on the priority summary.

[0046] *In order to prevent head of line blockage of the packet having a high priority in the first source FIFO 310 by the packet having a low priority in the first packet FIFO 330, the scheduler 360 would queue the first [low priority] packet FIFO 330 to be processed first.* (Emphasis added.)

In other words, as determined from the priority summary, the scheduler 360 schedules a lower priority packet within an n packet FIFO *before* a higher level priority packet within an n packet FIFO.

In one embodiment of the present Application:

[0044] This [*i.e.*, the scheduler 360] would queue the first (low priority) packet FIFO 330 to be processed first] would allow the packet having the low priority in the first packet FIFO 330 to be transferred to the destination FIFO 336. Then, the packet having a high priority would be transmitted toward the first packet FIFO 330 and the first packet FIFO 330 would be processed next. *Thus, the head of line blockage is avoided.* (Emphasis added.)

However, unlike the invention of Claim 1, Dell arbitrates between packets based on priority such that packets in a FIFO *that contain the highest priority are always processed before packets in other FIFOs.* (See Examiner's Action, page 3; emphasis added.) In Claim 1, however, the priority summarizer *also* prioritizes for an n packet FIFO *that is to receive a highest priority packet*, which is not disclosed or suggested in Dell. In at least some embodiments of the present specification, for example, the n packet FIFO that *is to receive* the highest priority packet is prioritized higher than other n packet FIFOs.

Nor has the Examiner cited the other references of Lo and Lee as curing the deficiencies of Dell regarding a priority summarizer as claimed in Claim 1. Therefore, the Examiner has not presented a *prima facie* case of rejection of Claim 1. In view of the foregoing remarks, the cited references do not support of the Examiner's rejection of independent Claim 1, nor for similar reasons

the rejection of independent Claim 8 and Claim 15, nor their dependent claims, when considered as a whole. Therefore, Claims 3-8, 10-15, and 17-20 are nonobvious over the cited references under 35 U.S.C. §103(a). The Applicant therefore respectfully requests the Examiner withdraw the rejection of Claims 1, 3-8, 10-15, and 17-20 and allow issuance thereof.

II. Conclusion

In view of the foregoing amendment and remarks, the Applicant now sees all of the Claims currently pending in this Application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1, 3-8, 10-15, and 17-20. Furthermore, the Applicant reserves the right to address arguments and positions in the Examiner's Action at a later date that are not addressed in the present Amendment.

The Applicant requests the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present Application. The Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account 08-2395.

Respectfully submitted,

HITT GAINES, P.C.

A handwritten signature in black ink, appearing to read 'D. Hitt', is written over a horizontal line.

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